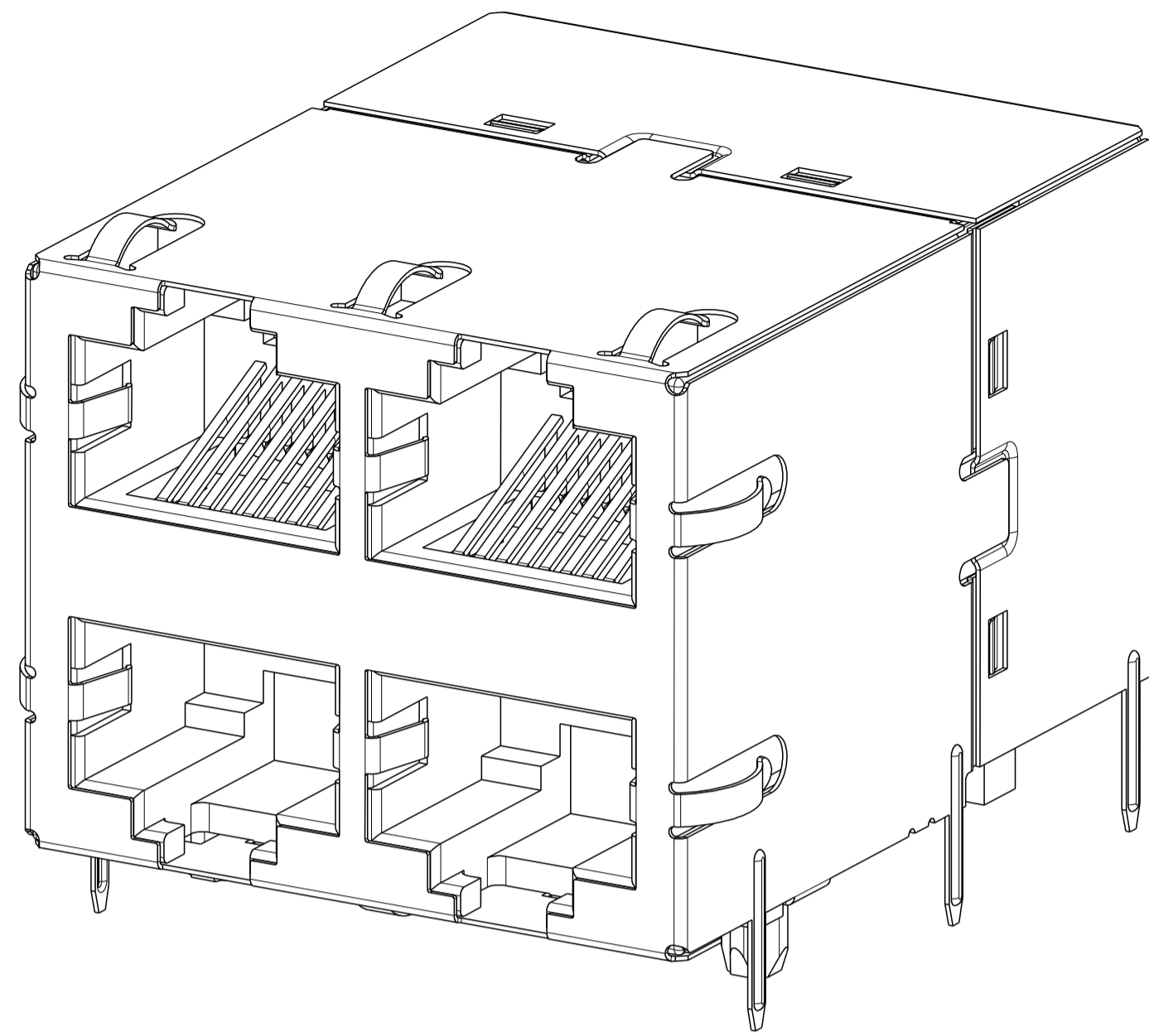


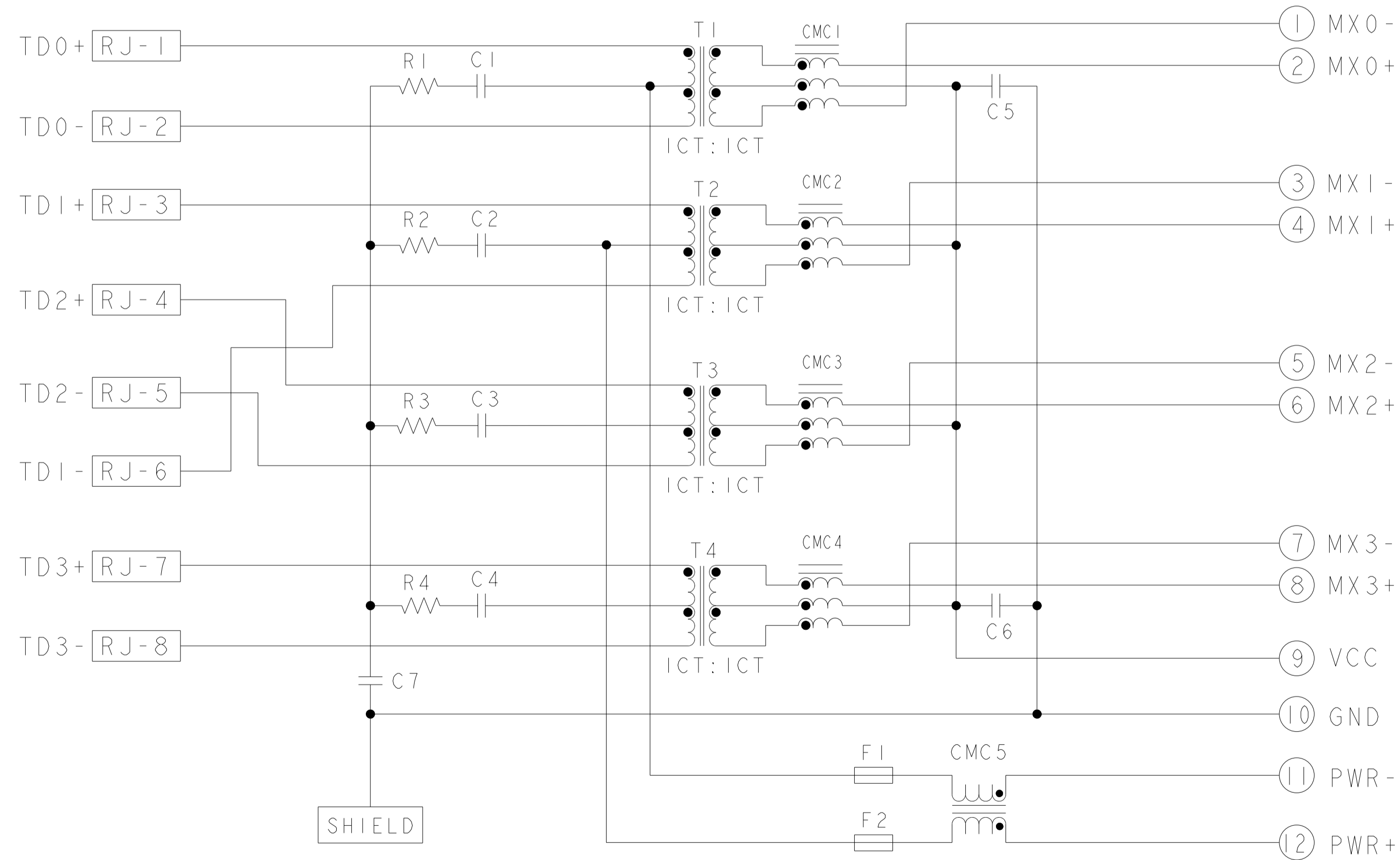
THIS DRAWING AND THE SUBJECT MATTER SHOWN THEREON ARE CONFIDENTIAL AND THE PROPERTY OF BEL/STEWART/TRP CONNECTOR AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN ANY MANNER WITHOUT THE WRITTEN CONSENT OF TRP CONNECTOR.

PRODUCT MAY BE PROTECTED BY ONE OR MORE OF THE FOLLOWING US PATENTS:  
 5736910 5939955 6425781 6428361 6554638 6840817 7123117  
 7429195 7717749 7808751 6217391 6149050 7924130

REVISIONS					
P	LTN	DESCRIPTION	DATE	DWN	APVD
2		EC-1411035 COMPANY LOGO CHANGE	18DEC2014	GZ	TY



S9HG153ET GIGABIT POE PLUS CIRCUIT  
 TOP AND BOTTOM PORTS

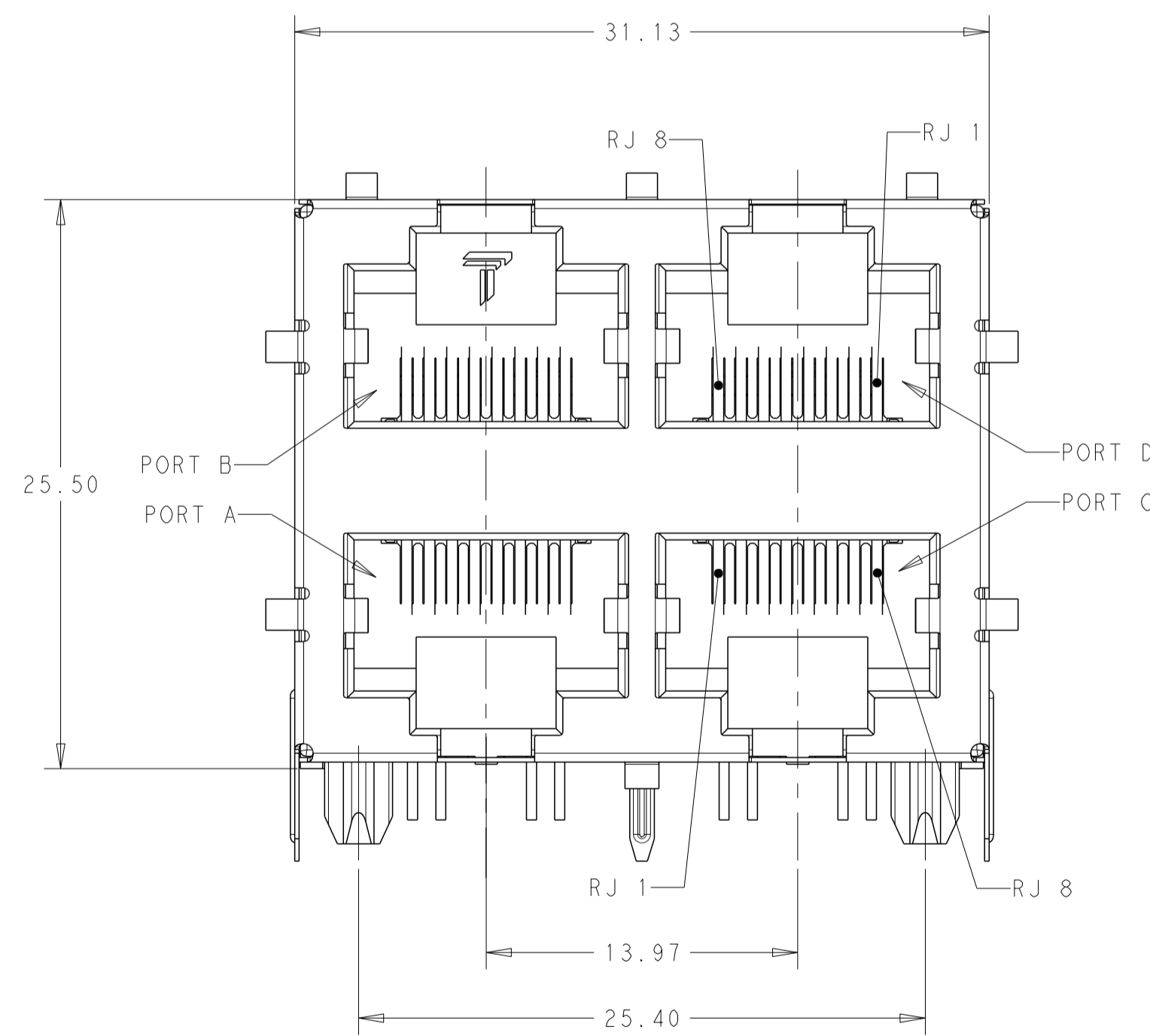
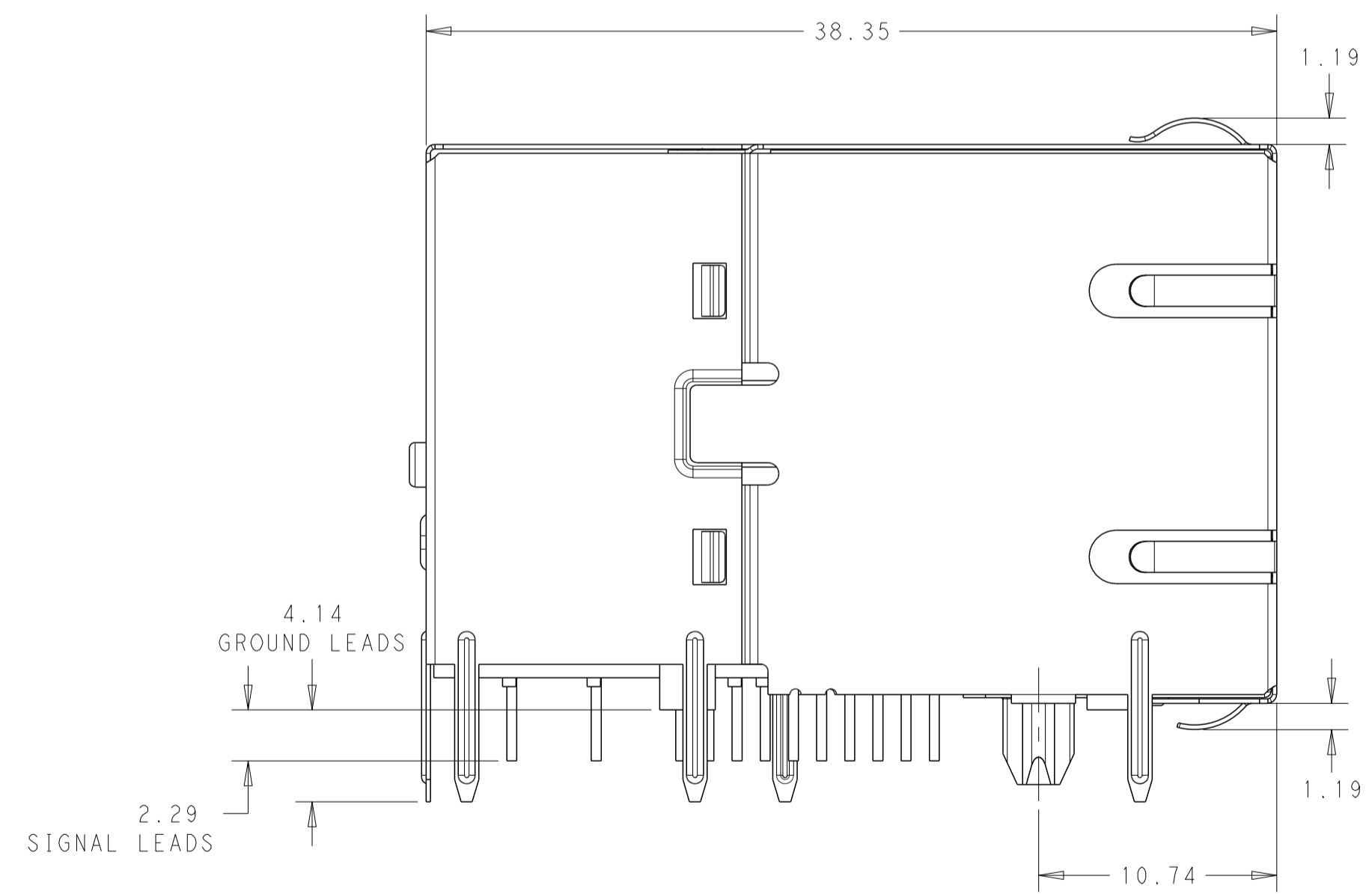
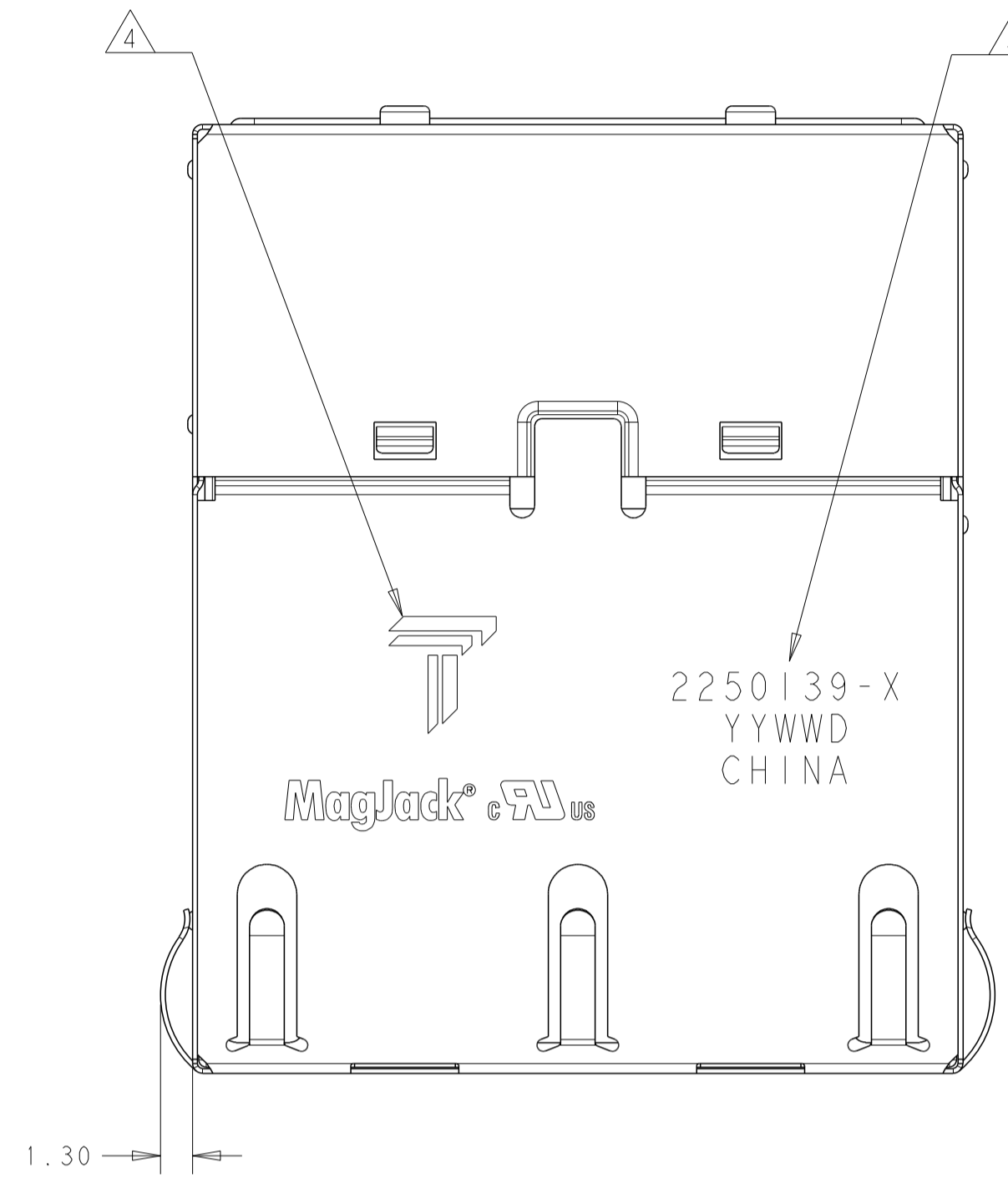


R1-R4 = 75Ohms, 1/16 W, RESISTORS  
 C1-C4 = 22nF, 100V, CAPACITORS  
 C5 - C6 = 10nF, 50V, CAPACITOR  
 C7 = 1000pF, 2kV, DECOUPLING CAPACITOR  
 F1-F2 = 63V, 1.5A, FUSES

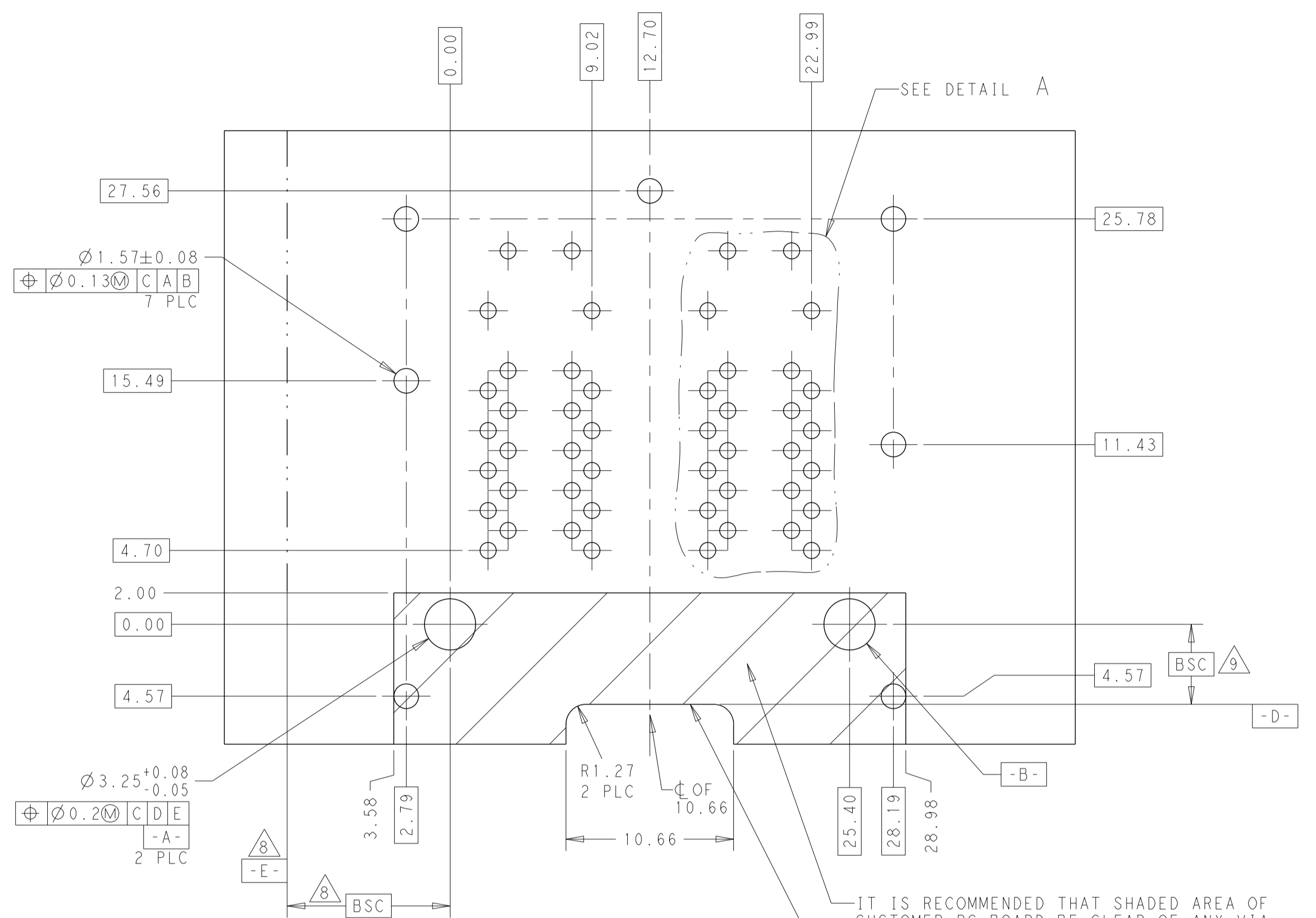
1. MATERIALS:  
 PLASTIC HOUSING: BLACK, THERMOPLASTIC FLAMMABILITY RATING UL 94V-0  
 SHIELD: BRASS, PREPLATED WITH 0.76um MIN SEMI-BRIGHT NICKEL,  
 POST DIPPED WITH 2.54um MIN SAC SOLDER OR PURE TIN SOLDER DIP  
 ON SOLDER TAILS,  
 CONTACTS: PHOSPHOR BRONZE, 1.27um MIN OVERALL NICKEL  
 UNDERPLATE WITH SELECT 1.27um MIN GOLD OR WITH SELECT 0.05um MIN  
 GOLD OVER 0.76um MIN PALLADIUM-NICKEL AT MATING INTERFACE AND  
 2.54um MIN MATTE TIN ON SOLDER TAILS.
2. MAGNETICS  
 APPLICATION: 10/100/1000 BASE-T, PoE PLUS, EXTENDED TEMPERATURE  
 IMPEDANCE: 100 OHMS  
 TURNS RATIO (CHIP:CABLE): 1:1 ALL FOUR PAIRS  
 OPEN CIRCUIT INDUCTANCE (OCL): ALL CHANNELS  
 350uH MIN @100kHz, 0.1VRMS WITH 8mADC BIAS FROM -40°C TO +85°C,  
 120uH MIN @100kHz, 0.1VRMS WITH 19mADC BIAS FROM -40°C TO +85°C,  
 ACROSS RJ1-RJ2 & RJ3-RJ6  
 ALL FOUR PAIRS BI-DIRECTIONAL  
 POE CURRENT: 600mADC MAX  
 PERFORMANCE @ 25°C:  
 INSERTION LOSS (IL): 1.1dB MAX FROM 0.5MHz TO 100MHz  
 RETURN LOSS (RL): 18dB MIN FROM 0.5MHz TO 40MHz  
 12-20LOG(f/80)dB MIN FROM 40.1MHz TO 100MHz  
 CROSSTALK ATTENUATION: 35dB MIN FROM 0.5MHz TO 40MHz  
 33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz  
 COMMON MODE REJECTION RATIO (CMRR): 30dB MIN FROM 0.5MHz TO 100MHz  
 ISOLATION VOLTAGE: 2250VDC(MAX) FOR 60 SECONDS WITH A RISE TIME OF  
 500V/SEC AND WITH ALL PORTS CONNECTED.
3. PART NUMBER, DATE CODE AND COUNTRY OF ORIGIN ARE  
 LOCATED IN APPROXIMATE AREA SHOWN.  
 DATE CODE: YYWWD WHERE "YY" IS YEAR, "WW" IS WORK WEEK, "D" IS DAY  
 OF WEEK, WITH SUNDAY =1
4. TRP CONNECTOR LOGO AND AGENCY APPROVAL LOGO ARE  
 LOCATED IN APPROXIMATE AREA SHOWN.
5. OPERATING TEMP: FROM -40°C TO +85°C.
6. RJ45 CAVITY CONFORMS TO FCC RULES AND REGULATION PART 68 SUBPART F.
7. INDICATED MAGNETIC CONNECTIONS ARE SYMMETRICAL AND  
 SUPPORT AUTO-MDI/MDIX.
8. DATUM AND BASIC DIMENSION ESTABLISHED BY CUSTOMER.
9. BASIC DIMENSION ESTABLISHED BY CUSTOMER, BUT MAY NOT BE  
 GREATER THAN 5.08mm.
10. THE PARTS ARE RECOMMENDED FOR WAVE SOLDERING PROCESS,  
 PEAK TEMPERATURE 260°C MAX, 10 SECONDS MAX.

2250139-1  
 PART NUMBER

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN: 23DEC2013 TOMMY REN/TERREY LIN			DONGGUAN CHINA
DIMENSIONS: mm		CHK: 23DEC2013 TOMMY REN			
		TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ± 4 PLC ± ANGLES ± APPLICATION SPEC ±		MODEL NAME: MAGJACK STACK PoE+	
PRODUCT SPEC: 108-104004		APVD: 23DEC2013 KEITH ZHU		DESC: 2X2 S9HG153ET GIGABIT PoE+ W/O LED	
		CUSTOMER DRAWING		SIZE: A1 CAGE CODE: C=2250139 DRAWING NO: 2250139 SCALE: 4:1 SHEET 1 OF 3 REV 2	

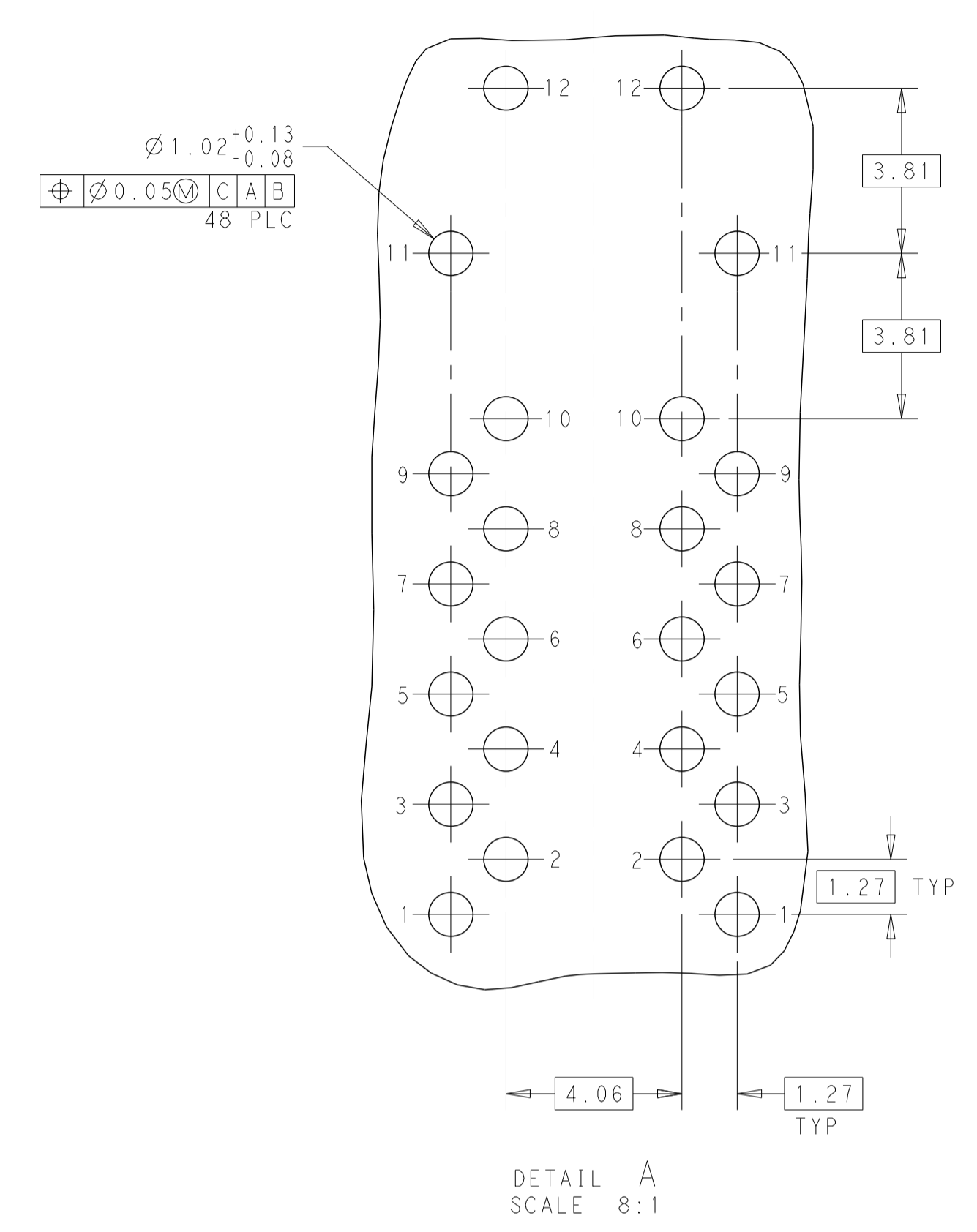


THIS DRAWING IS A CONTROLLED DOCUMENT.		DRW: TOMMY REN / 23DEC2013	 <b>trp</b> CONNECTOR <small>a bel group</small>	DONGGUAN CHINA
		CHK: TOMMY REN / 23DEC2013		
		APP: KEITH ZHU / 23DEC2013		
DIMENSIONS: mm		TOLERANCES UNLESS OTHERWISE SPECIFIED:	MODEL NAME	DESC: 2X2 S9HG153ET GIGABIT PoE+ W/O LED
		0 PLC ±0.25	MAGJACK	SIZE: A1
PRODUCT SPEC: 108-104004		1 PLC ±0.25	STACK PoE+	CAGE CODE: C=2250139
		2 PLC ±0.25	CUSTOMER DRAWING	DRAWING NO: 2250139
		3 PLC ±0.25		SCALE: 4:1
		4 PLC ±		SHEET: 2 OF 3
		ANGLES ±		REV: 2
		APPLICATION SPEC ±		

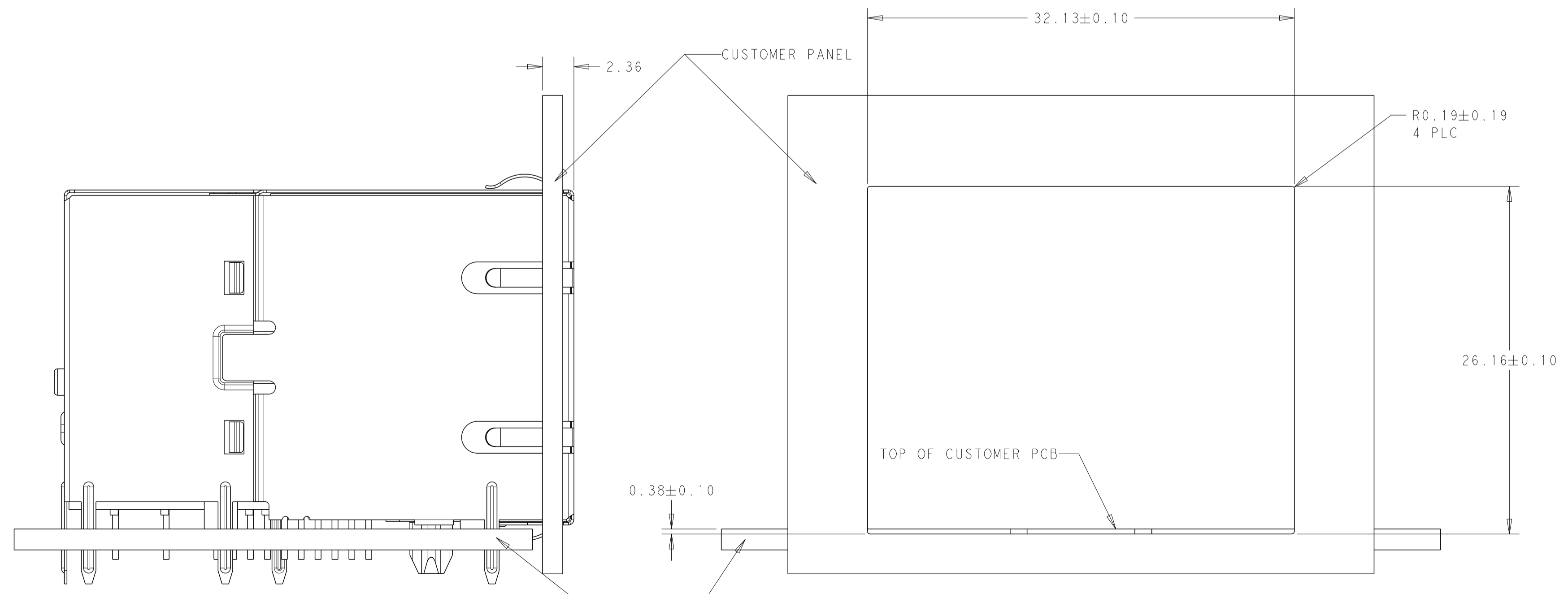


RECOMMENDED PCB LAYOUT COMPONENT SIDE VIEW

IT IS RECOMMENDED THAT SHADED AREA OF CUSTOMER PC BOARD BE CLEAR OF ANY VIA HOLE, COMPONENT AND CIRCUIT TRACE  
 RECOMMENDED PCB FRONT EDGE CUTOUT: THE BOTTOM SHIELD GROUND TABS(FRONT) SHOULD NOT BE SEATED ON THE TOP OF THE PCB

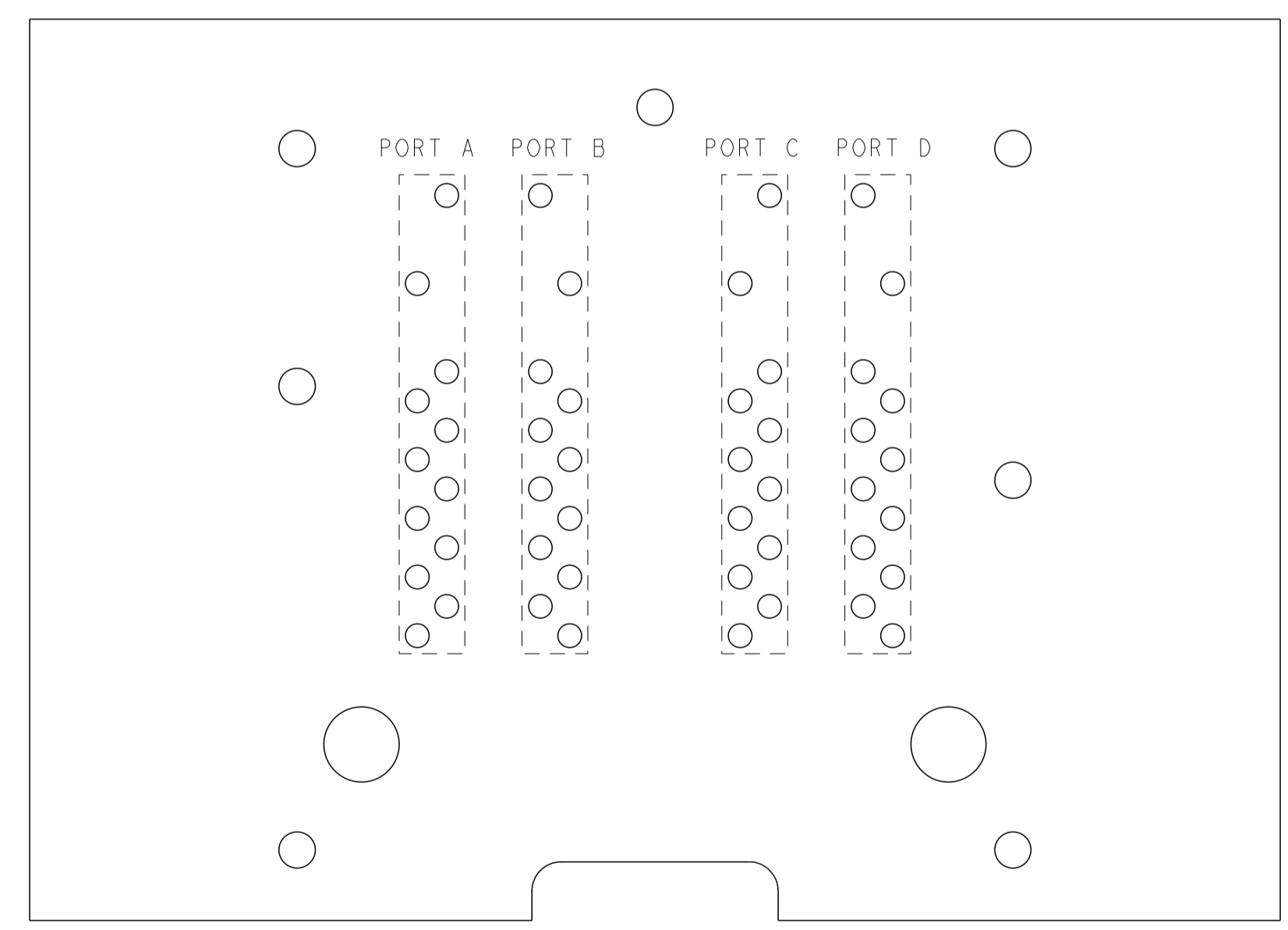


DETAIL A SCALE 8:1



SHOWN WITH PANEL AND CUSTOMER PCB ASSEMBLY

SUGGESTED PANEL CUTOUT DIMENSIONS



PORT ASSIGNMENT COMPONENT SIDE VIEW

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWG: 23DEC2013 TOMMY REN/TEREY LIN			DONGGUAN CHINA
DIMENSIONS: mm		CHK: TOMMY REN 23DEC2013			
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APPROV: KEITH ZHU 23DEC2013		DESC: 2X2 MAG45(TM), GIGABIT S9HG153ET	
		0 PLC ± 1 PLC ± 2 PLC ±0.25 3 PLC ± 4 PLC ± ANGLES ± APPLICATION SPEC ±		MODEL NAME: model_name1 model_name2	
PRODUCT SPEC		SCALE: NTS		SIZE: A1 CAGE CODE: 2250139 DRAWING NO: 3 OF 3 REV: 1	
CUSTOMER DRAWING		SCALE: NTS		SHEET 3 OF 3 REV 1	